Searching for: (interconnect and probabilistic and test and design and programmable and chip) (start a new search)

Found **42** within *The ACM Guide to Computing Literature* (Bibliographic citations from major publishers in computing)

Limit your search to Publications from ACM and Affiliated Organizations (Full-Text collection: **312,030** items)

REFINE YOUR SEARCH

Refine by Keywords

Discovered Terms

Refine by People
Names
Institutions
Authors
Reviewers

Refine by Publications
Publication Year
Publication Names
ACM Publications
All Publications
Content Formats
Publishers

Refine by Conferences
Sponsors
Events
Proceeding Series

ADVANCED SEARCH

Advanced Search

FEEDBACK

Please provide us with feedback

Found **42** of **1,697,209**

Search Results Related Journals Related SIGs

Results 1 - 20 of 42

Sort by relevance in expanded form

Result page: **1** 2 3 next

1 Via-configurable routing architectures and fast design mappability estimation for regular fabrics

Y. Ran, M. Marek-Sadowska

May 2005 **ICCAD '05:** Proceedings of the 2005 IEEE/ACM International conference on Computer-aided desi

Publisher: IEEE Computer Society

Full text available: Pdf (366.95 KB)

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 15, Downloads (Overall): 136, Citation Count: 4

In this paper, we describe a new via-configurable routing architecture which shows much better throughput anc performance than the previous structures. We demonstrate how to construct a single-via-mask fabric to reduce further the mask cost, and we analyze ...

2 Recent developments in high-level synthesis

Youn-Long Lin

January 1997 **Transactions on Design Automation of Electronic Systems (TODAES)** , Volume 2 Issue

Publisher: ACM Request Permissions

Full text available: Pdf (232.47 KB)

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 62, Downloads (Overall): 2296, Citation Count:

We survey recent developments in high level synthesis technology for VLSI design. The need for higher-level design automation tools are discussed first. We then describe some basic techniques for various subtasks of hig level synthesis. Techniques that ...

Keywords: VLSI design, design automation, design methodology, high level synthesis

3 Active leakage power optimization for FPGAs

Jason H. Anderson, Farid N. Najm, Tim Tuan

February 2004 **FPGA '04:** Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmal gate arrays

Publisher: ACM Request Permissions

Full text available: Pdf (214.96 KB)

Bibliometrics: Downloads (6 Weeks): 6, Downloads (12 Months): 30, Downloads (Overall): 359, Citation Count: 2€

We consider active leakage power dissipation in FPGAs and present a "no cost" approach for active leakage reduction. It is well-known that the leakage power consumed by a digital CMOS circuit depends strongly on the state of its inputs. Our leakage reduction ...

Keywords: FPGAs, field-programmable gate arrays, leakage, low-power design, optimization, power

4 On metrics for comparing routability estimation methods for FPGAs

Parivallal Kannan, Shankar Balachandran, Dinesh Bhatia

June 2002 **DAC '02:** Proceedings of the 39th annual Design Automation Conference

Publisher: ACM Request Permissions

Full text available: Pdf (226.17 KB)

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 9, Downloads (Overall): 242, Citation Count: 9

Interconnect management is a critical design issue for large FPGA based designs. One of the most important iss for planning interconnection is the ability to accurately and efficiently predict the routability of a given design o given FPGA architecture. ...

Keywords: FPGA, RISA, congestion, fGREP, rent's rule, routability estimation